IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re the application of:
HENRY CHUNG

Docket: 30-4718 (4780)

Serial Number: 09/328,645

Group Art Unit: 2811

Filed: June 9, 1999

Examiner: H. Vu

For: A FABRICATION METHOD OF INTEGRATED CIRCUITS WITH BORDERLESS VIAS AND LOW DIELECTRIC-CONSTANT INTER-METAL DIELECTRICS

BRIEF FOR APPELLANT

Commissioner for Patents
Washington, D.C. 20231

Sir:

This is an Appeal to the Board of Patent Appeals and Interferences from the Final Rejection of claims 5-7 mailed December 4, 2002 in the above identified case. A Notice of Appeal was filed on March 3, 2002. An oral hearing is not requested.

This Brief is hereby filed in triplicate. The Commissioner is authorized to charge the required appeal brief fee of $320.00 to Deposit Acct. No. 01-1125. In the event that the Commissioner determines that an additional extension of time is required in order for this submission to be timely, it is requested that this submission include a petition for an additional extension for the required length of time and the Commissioner is authorized to charge any other fees necessitated by this paper to Deposit Acct. No. 01-1125.

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I. REAL PARTY IN INTEREST

The real party in interest is Honeywell International, Inc., which changed its corporate name from AlliedSignal, Inc, the assignee of record.

II. RELATED APPEALS AND INTERFERENCES

With respect to other appeals or interferences that will directly affect, or be directly affected by, or have a bearing on the Board's decision in this appeal, please note that there are no other related applications on appeal or subject to an interference known to appellant, appellant's legal representative or the assignee.

III. STATUS OF CLAIMS

The claims in the application are 1-16. Claims 5-7 are pending, stand rejected and are on appeal. Claims 1-4, and 8-16 have been withdrawn from consideration. No claims are allowed.

IV. STATUS OF AMENDMENTS

A response was filed on January 6, 2003, after final rejection, however the response did not place the application in condition for allowance. No amendments were submitted after final rejection.

V. SUMMARY OF THE INVENTION

The present invention claims an integrated circuit structure. The structure includes a substrate; a layer of a first polymeric dielectric material on the

substrate; a plurality of spaced apart metal contacts on the layer of the first polymeric dielectric material; a space between adjacent metal contacts, each space being filled with a second polymeric dielectric material; a recess in the filled spaces of the layer of the second polymeric dielectric material extending from a level at a top of the metal contacts a part of the distance toward the substrate; an additional layer of the first polymeric dielectric material on at least some of the metal contacts and in the recesses on the filled spaces of the second polymeric dielectric material such that there is optionally a gap in at least one of the recesses of the additional layer of first polymeric dielectric material at a side wall of a metal contact; and at least one via extending through the additional layer of the first polymeric dielectric material extending to the top of at least one of the metal contacts and optionally to said gap; wherein the first dielectric material and the second dielectric material have substantially different etch resistance properties.

VI. ISSUES

(a) Whether claims 5-7 are unpatentable under 35 U.S.C. 102 over Lu et al.

VII. GROUPING OF CLAIMS

Appellants submit that the claims of this invention do not stand or fall together. Rather, they stand or fall in the separate groups listed below:

Group I: Claims 5 and 6. Claim 5 is drawn to integrated circuit structure, and Claim 6 is drawn to this circuit structure further comprising a via which is filled with at least one metal.

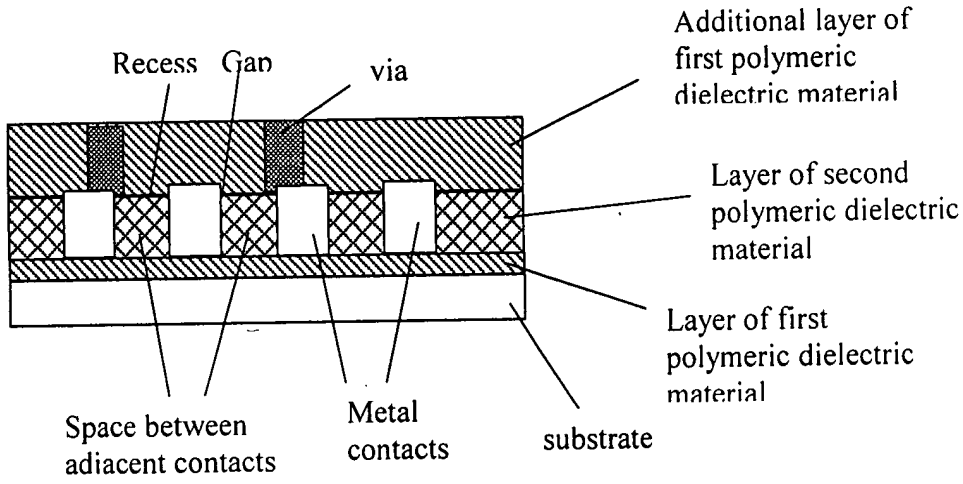
Group II: Claim 7, drawn to an integrated circuit structure having a first polymeric dielectric material which is organic and a second polymeric dielectric material which is inorganic. This claim describes the physical makeup of components of the circuit, not just the circuit's structure.

VIII. ARGUMENTS

The Examiner rejected claims 5-7 under 35 U.S.C. 102 as being unpatentable over Lu et al. Appellants respectfully submit that this ground of rejection is improper.

The present invention relates to integrated circuits and the like. More particularly, the invention relates to the formation of borderless vias in intermetal dielectrics. The invention claims an integrated circuit structure which comprises a substrate and a layer of a first polymeric dielectric material on the substrate, and a plurality of spaced apart metal contacts on the layer of the first polymeric dielectric material. A space is present between adjacent metal contacts, each space being filled with a second polymeric dielectric material. A recess is present in the filled spaces of the second polymeric dielectric material extending from a level at a top of the metal contacts a part of the distance toward the substrate. An additional layer of the first polymeric dielectric material is also present on at least some of the metal contacts and in the recesses on the filled spaces of the second polymeric dielectric material such that there is optionally a gap in at least one of the recesses of the additional layer of first polymeric dielectric material at a side wall of a metal contact. The integrated circuit structure also comprises at least one via extending through the additional layer of the first polymeric dielectric material

extending to the top of at least one of the metal contacts and optionally to said gap. This via may be filled with at least one metal. It is an important feature of the invention that the first dielectric material and the second polymeric dielectric material have substantially different etch resistance properties. In a preferred embodiment, the first polymeric dielectric material is organic and the second polymeric dielectric material is inorganic. The invention may be schematically represented as follows:



Lu et al. also relates to the formation of integrated circuit dielectrics. In particular, it describes a surface treatment for silica xerogel dielectrics, for enhancing the adhesion of overlying layers. Lu et al. describe various embodiments for the formation of integrated circuits as underlying layers for their invention. The examiner is of the position that the teachings of Lu et al. anticipate the claimed invention, particularly pointing out Figs. 1(g) and 2(b) of Lu et al. Appellants urge that this is not the case, since Lu et al. fail to teach several key features of the present invention.

Indeed, Lu et al. teach some layers and/or features of the presently claimed invention. However, Appellants respectfully submit that Lu et al. fails to teach the circuit structure as claimed by the present invention.

As stated above, the present invention teaches a layer of a *first* polymeric material having spaced apart metal contacts thereon. A layer of a *second* polymeric material is deposited *between* the contacts and *on* the first polymeric material, as shown in the Figures. Recesses in the layer of the second polymeric dielectric material are formed at the top of the filled spaces. The recesses and at least some of the metal contacts are then applied with an *additional layer* of the *first* polymeric dielectric material. However, such is not taught by Lu et al. That is, Lu, et al do not apply an *additional layer* of the *first* polymeric dielectric material on at least some of the metal contacts and in the recesses on the filled spaces of the second polymeric dielectric.

Indeed, Lu et al. teaches a substrate 102 having a first dielectric layer 120 thereon. The first dielectric layer 120 as shown in Fig. 1(g). Lu et al. then spin-coats an oxide liner 140 (a second dielectric layer) onto the top surface of the dielectric layer 120. The oxide liner is then provided with metal interconnects 130 formed on liner 140. The spaces between the oxide liner coated metal interconnects 130 are filled with a xerogel 142 (a third dielectric layer), which may include recesses at the top of the xerogel 142 as shown in Fig. 1(g). A layer of hydrogen silsesquioxane (HSQ) 144 (a fourth dielectric) is then deposited on top of the layer 142 and in the recesses. An additional dielectric layer 146 is applied on top of the HSQ layer 144. Lu et al. does not teach that this additional dielectric layer 146 is present within the recesses between the interconnects.This recess is filled with hydrogen silsesquioxane which is used as an adhesion layer. Lu et al. also does not specify that dielectric layer 144 or 146 must be the same dielectric as

used in dielectric 120, as is required by the present invention. Thus, it is urged that Lu et al. fails to teach the requirement of "an additional layer of the first polymeric dielectric material on at least some of the metal contacts and *in the recesses* on the filled spaces of the sec*ond polymeric dielectric material*".

The examiner next points to Fig. 2b, stating that layers 272, 274 of Lu et al. correspond to the present additional dielectric layer in the recesses. Applicants respectfully urge that this is not the case. Indeed, Lu et al. teaches the formation of interconnects 260 on a dielectric layer 246, as shown in Fig. 2(b). Lu et al. then spin-coats an oxide liner (second dielectric) 270 onto the interconnects and the top surface of the dielectric layer 246. The spaces between the interconnects are filled with a xerogel 272 (third dielectric), which may include recesses at the top of the xerogel 272 as shown in Fig. 2(b). A layer of hydrogen silsesquioxane (HSQ) (fourth dielectric) 274 is then deposited on top of the layer 272 and in the recesses, as shown in Fig. 2(b). Yet additional dielectric layer 276 is applied on top of the HSQ layer 274. Lu et al. does not teach that this additional dielectric layer 276 is present within the recesses between the interconnects. Rather, this recess is filled with hydrogen silsesquioxane which is used as an adhesion layer. Lu et al. also does not specify that upper layer dielectric 274 which is in the recess, or 276 *must* be the same dielectric as used in dielectric 246, as is required by the presentclaims. Thus, it is again urged that Lu et al. fails to teach the requirement of "an additional layer of the first polymeric dielectric material on at least some of the metal contacts and *in the recesses* on the filled spaces of the sec*ond polymeric dielectric material*".

Lu et al. further fails to require or appreciate that the first and second dielectric materials which have substantially different etch resistant properties, for the formation of vias and trenches. Lu et al. also does not teach that the second

dielectric material which is *in contact with* the metal contacts and with the first dielectric material. Rather, the oxide layer 140 forms a barrier over the interconnects 130 and the dielectric 120. Likewise, the oxide layer 270 forms a barrier over the interconnects 260 and the dielectric 246.

Appellants respectfully urge that the cited reference's failure to teach the above mentioned key features of the present claims renders the present invention patentably distinct from Lu et al. Thus, for all the above reasons, Appellants respectfully submit that
claims 5-7 are patentable over the cited reference, and the 35 U.S.C. 102 rejection should be overruled.

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail, postage pre-paid in an envelope addressed to Commissioner for Patents and Trademarks, Washington D.C. 20231, on April 3, 2003.

Richard S. Roberts

IX. APPENDIX

5. An integrated circuit structure which comprises

(a) a substrate;

(b) a layer of a first polymeric dielectric material on the substrate;

(c) a plurality of spaced apart metal contacts on the layer of the first polymeric dielectric material;

(d) a space between adjacent metal contacts, each space being filled with a second polymeric dielectric material;

(e) a recess in the filled spaces of the layer of the second polymeric dielectric material extending from a level at a top of the metal contacts a part of the distance toward the substrate;

(f) an additional layer of the first polymeric dielectric material on at least some of the metal contacts and in the recesses on the filled spaces of the second polymeric dielectric material such that there is optionally a gap in at least one of the recesses of the additional layer of first polymeric dielectric material at a side wall of a metal contact;

(g) at least one via extending through the additional layer of the first polymeric dielectric material extending to the top of at least one of the metal contacts and optionally to said gap;

wherein the first dielectric material and the second dielectric material have substantially different etch resistance properties.

6. The integrated structure of claim 5 wherein the via is filled with at least one metal.

7. The structure of claim 5 wherein the first polymeric dielectric material is organic and the second polymeric dielectric material is inorganic.